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CMOS Analog Multipliers: Low Power Design Strategies and the Impact of Threshold Voltage Variations

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Abstract

Due to process variations in key MOSFET parameters like channel length, width, threshold voltage (V_{th}) etc. the output of analog circuits is affected to a large extent. In this work, our aim is to examine the yield of a typical CMOS analog multiplier designed at 65 nm technology node due to V_{th} variations and figure out the variation in key parameters by using Gaussian distribution - Monte Carlo model. We have considered a typical Quad multiplier configuration to examine the variability in the multiplier output under 2% and 5% variation in threshold voltage of the 65 nm bulk BSIM model. Using the case of Gaussian distribution - Monte Carlo simulation, the standard deviation in the multiplier output is found to be 1.4 mV for both 2% and 5% variations. A good yield prediction with variation of 2% and 5% in V_{th} is possible at 65 nm technology node.

Keywords: *CMOS analog multipliers, Analog circuits, Process variations, Reliability, Monte Carlo models*

1.0 Introduction

Analog multiplier is one of the most important blocks in VLSI and communication systems e.g., frequency modulator, frequency shifter, adaptive filtering, phase detector, mixer etc. The main aim of a multiplier is to achieve the real time product of two continuous signal at the output. The conventional multiplier circuit consists of a typical electronic device for processing the input signal followed by an error minimization circuit which is caused by nonlinearity of the electronic device characteristic. The cancellation of nonlinearity is achieved by a typical differential circuit structure[1]. Analog multipliers can be designed by using the non-linear characteristics of MOSFET and it is a popular choice due to the rapid advancement in CMOS technology. It can be designed either in the subthreshold region (exponential) triode region or the saturation region (quadratic) of a MOSFET. Widely used CMOS multipliers, and their transistor level implementations have been discussed in detail[2]. A four quadrant CMOS analog multiplier has been designed using a Gilbert's six-transistor cell (GSTC)[3]. A compact four quadrant CMOS analog multiplier with wide voltage range has been discussed[4]. Design of CMOS transconductance multipliers have been discussed by Gunhee Han and Edgar S´anchez-Sinencio[5]. Chunhong Chen and Zheng Li proposed a multiplier circuit with an attempt to reduce the power consumption by operating all PMOSs in saturation region and NMOSs in the linear region[1]. Square law characteristics can be exploited in designing four quadrant multipliers by operating the MOS transistor in saturation region[6]. Significant improvement in linearity is reported in this design by using floating point inputs. Four-quadrant multiplier designed with

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single ended input is used to reduce the complexity of pre-processing circuit, power consumption and area[7]. Current differencing buffered amplifier finds huge applications in various high speed and large bandwidth applications due to its differential nature and simplicity[8,9]. Novel current differencing buffered amplifier is presented for realization of multiplier with single-ended output[10]. This design reduces the complexity of multiplier and maintains the operational performance. Dual translinear loop based current mode multiplier and divider circuit is presented at 0.35 µm CMOS technology node[11]. This circuit is based on squarer circuit and provides high speed, high linearity, low power consumption and 1.1% DC offset error. Tohid Aghaei and Ali Naderi Saatlo presented another method of designing CMOS analog multiplier consisting of two identical pairs of translinear loop. Due to symmetrical configuration, this circuit is capable of minimizing the error by the compensating squarer circuits which results in greater precision[12]. Current mode four-quadrant amplifier based on translinear current squarer provides control for enhanced input range and exhibits better linearity and higher robustness to process variation in standard CMOS technology[12]. Dynamic threshold voltage scheme allows the design of multiplier with lower supply voltage thereby reducing the total power consumption. This design is not affected by body effect and occupies minimal area[14]. In the following sections, first the theory and design of the designed analog multiplier at 65 nm will be discussed followed by the results that include reliability issues due V_{th} variations.

2.0 Theory and Design

Ideally the output of multiplier is just the multiplication of two different input signals. For multiplying two or more signals it is required to pass those signals from non-linear elements or it can be said that the signals have to be passed from a device having non-linear I-V characteristics. Initially, the analog multipliers were designed by using bipolar junction transistors (BJTs). Here, the exponential behaviour of current with respect to voltage of the BJT leads to an output which is a nonlinear function of the input signals. Currently, analog multiplier designs by using CMOS approach faces challenges mainly in the low power design[12,15]. In this work, we design an analog multiplier with four transistors (multiplying quad) using the CMOS technology at 65 nm. At the output end of the multiplying Quad, due to the non-linear characteristics of the MOSFET there are some higher order terms. So, the key challenge here is to filter out these higher order terms to get an ideal multiplier output.

To design a multiplier circuit, it is important to design multiplying Quad consisting of four transistors, a dual output mode operational amplifier (op-amp) and a biasing circuit is used to bias theop-amp. The proper size selection for for MOSFETs in the multiplying Quad, so that they can operate in triode region is an extremely crucial part of the design. The output of multiplieris classified based on the four quadrants. For bipolar input signals, it is essential to design four quadrant multipliers.

MOSFET can be operated in triode or saturation region. As discussed, we choose the triode operating region to perform the multiplication. We have to connect two different input signals V_x and V_y to the circuit. These inputs are bipolar or unipolar based on the application. In this work we choose both signals as bipolar signals. For designing input circuitry, we have to connect DC supply with the input signals. Drain and gate of the MOSFETs in the Quad multiplier are connected with the differential arrangement of voltage levels. Due to variation in supply, there will be a variation in drain output current. As we can see in drain current equation of MOSFETS in the triode regions as mentioned below which includes input voltage signals, threshold voltages and gate to source voltages[16].

$$I_{d1} = \mu_0 C_{ox} W/L \times (V_{gs} - V_t + V_y/2)\ (V_x/2) - \tfrac{1}{2}(V_x/2)^2 \quad \ldots (1)$$

$$I_{d2} = \mu_0 C_{ox} W/L \times (V_{gs} - V_t - V_y/2)\ (-V_x/2) - \tfrac{1}{2}(V_x/2)^2 \ldots (2)$$

$$I_{d3} = \mu_0 C_{ox} W/L \times (V_{gs} - V_t - V_y/2)\ (V_x/2) - \tfrac{1}{2}(V_x/2)^2 \quad \ldots (3)$$

$$I_{d4} = \mu_0 C_{ox} W/L \times (V_{gs} - V_t + V_y/2)\ (-V_x/2) - \tfrac{1}{2}(V_x/2)^2 \ldots (4)$$

As we already discussed to get the ideal output expression, we must represent final output in the form of KV_xV_y. Where K is the scaling factor, and V_x and V_y are the inputs. To achieve this, it is important that all four MOSFETs (M1-M4) in the Quad multiplier as shown in Fig.1 have the same threshold voltages. Now the important task is to maintain source voltage to be the same for all four MOSFETs to prevent changes due to the body effect. The drain current equation consists of several other parameters like threshold voltage, Vgs (gate to source voltage) etc. as we can see in representation of the drain current. So to represent output in the form of multiplication of two signals and to filter out higher order terms and common voltage like the threshold voltage we have to design an additional circuit. In this work we design an op-amp having feedback resistance which converts these currents into voltages. Then at the output end we can represent our output in the form of difference of two voltages. So now for proper design of the analog multiplier we have to perform three important tasks, one is to convert current into voltage, second to maintain source of all MOSFETs at the same voltage or common mode voltage and the last to provide proper differential circuit. Dual output mode op-amp is the single solution of all those requirements mentioned above.

An op-amp is designed at 65 nm technology to provide a common mode voltage at the output end which connects with

the sources of MOSFETs (M1-M4) in the Quad multiplier circuit. Choosing a proper value of common mode voltage is one of the challenges in designing of such an op-amp. A proper value of source voltage required to make all MOSFETs in the Quad multiplier circuitto operate in triode region, the condition is $(V_{gs}\text{-}V_{th})>V_{ds}$ and $V_{gs}>V_{th}$. If we choose higher value of common mode voltage, it creates difficulty in biasing the MOSFETs in the triode region. And for lower value of common mode voltage limits the swing or output voltage range. So, an intermediate value for proper operation must be chosen.

We connect Quad multiplier with op-amp in such a manner that entering currents into the two input terminals of op-amp can be represented as,

$$I_{+} = (I_{d1}+I_{d2}) \quad \text{... (5)}$$

$$I_{-} = (I_{d3}+I_{d4}) \quad \text{... (6)}$$

I_{+} and I_{-} are those currents which are entering into non-inverting and inverting terminals of the op-amp. By proper selection of the feedback resistance, the desired output voltage can be obtained. An additional circuit is also required to provide biasing to the op-amp. When the current enters the op-amp from feedback resistance, there will be a voltage at inverting and non-inverting end. At the output end we can get the proper different equations between these two voltages by selecting proper values of resistance. As we assume that threshold voltage of all MOSFETSsare the same.

After the cancellation of the common term in equations (1-4), output is the multiplication of input voltages. Due to elimination of higher order terms, we get highly linear multiplier characteristics.

We can express our output as,

$$V_{out} = R\,(I_{+}-I_{-}) \quad \text{... (7)}$$

$$V_{out} = R\mu_0 C_{ox} W/L(V_x/2\times V_y/2)+(-V_x/2-V_y/2) -(-V_x/2\times V_y/2)(V_x/2\times V_y/2) \quad \text{... (8)}$$

$$V_{out} = R\mu_0 C_{ox} W/L\times V_x V_y \quad \text{... (9)}$$

where R is the feedback resistor (R5/R6).

Fig.1 shows the complete circuit diagram which consists of three blocks, CMOS analog multiplier with CMOS operational amplifier and the biasing circuit. The design of the CMOS analog multiplier circuit is based on the specifications

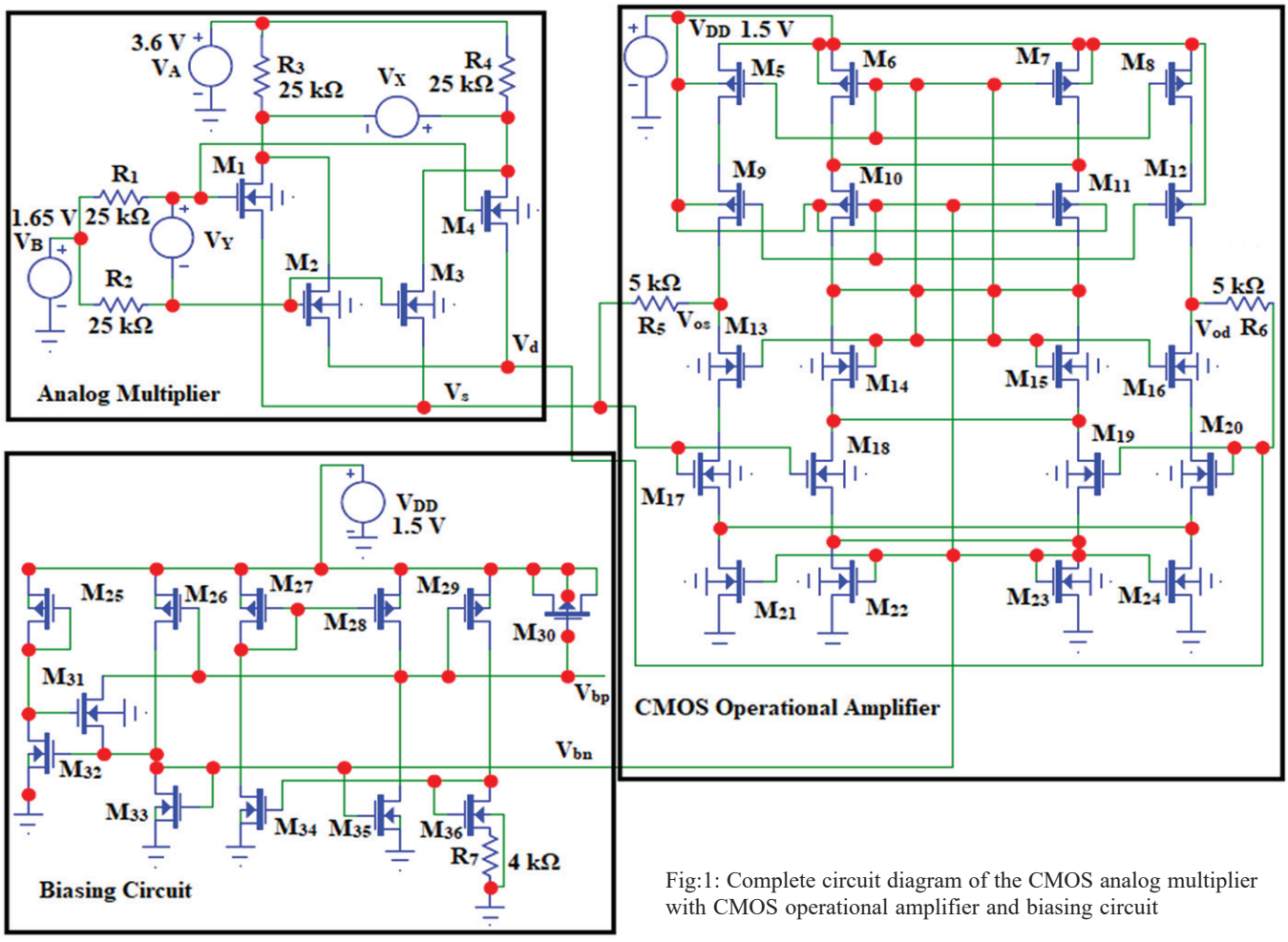

Fig:1: Complete circuit diagram of the CMOS analog multiplier with CMOS operational amplifier and biasing circuit

Table-1: W/L of MOSFETS used in the design of the complete CMOS analog multiplier

MOSFET	W(um)/L(um)	MOSFET	W/L	MOSFET	W/L	MOSFET	
M1	16.25/3.25=5	M10	2.6/0.13=20	M19	1.3/0.13=10	M28	2.6/0.26=10
M2	16.25/3.25=5	M11	2.6/0.13=20	M20	1.3/0.13=10	M29	1.3/0.13=10
M3	16.25/3.25=5	M12	2.6/0.13=20	M21	1.3/0.13=10	M30	13/13=1
M4	16.25/3.25=5	M13	1.3/0.13=10	M22	1.3/0.13=10	M31	1.3/0.13=10
M5	2.6/0.13=20	M14	1.3/0.13=10	M23	1.3/0.13=10	M32	1.3/0.13=10
M6	2.6/0.13=20	M15	1.3/0.13=10	M24	1.3/0.13=10	M33	1.3/0.13=10
M7	2.6/0.13=20	M16	1.3/0.13=10	M25	2.6/0.13=20	M34	1.3/0.26=5
M8	2.6/0.13=20	M17	1.3/0.13=10	M26	2.6/0.13=20	M35	1.3/0.26=5
M9	2.6/0.13=20	M18	1.3/0.13=10	M27	2.6/0.26=10	M36	5.2/0.13=40

and design considerations presented in ref.[16,17]. MOSFETs M1 to M4 constitute the analog multiplier, MOSFETs M5 to M24 constitute the CMOS operational amplifier and the MOSFETs M25 to M36 constitute the biasing circuit. V_A and V_B are set to 3.6V and 1.65V respectively in the current simulation. Table 1 shows the W/L of MOSFETS used in the design of the complete CMOS analog multiplier.

3.0 Results

Reliability is a major concern for the design of analog integrated circuits. Reliability can be classified in two-part static reliability and dynamic reliability. In the current scenario, there is a continuous downscaling of the MOSFET to achieve low power operation and to reduce size of the electronic devices. When MOSFET size is in the nanoscale range it is challenging to fabricate analog circuits due to inter or intra die variations. At the time of fabrication due to variation in thickness of oxide, variation in threshold voltage etc. output of the analog circuit will be affected. This variation is permanent in nature and is known as static reliability. Static variation does not vary with time. So, at the time of fabrication if there are some variation in threshold voltage, it will affect the whole circuit performance for the entire lifetime of the circuit. So, it is very important to optimize the circuit against the variation in these process parameters. Fig.2 shows the output of the designed analog multiplier where varies from -1.0 to 1.0 V.

Quad multiplier output is dependent on threshold voltage. Due to variations in the threshold voltage, there will be a change in key output parameters. These effects become worse if variation is different in all the MOSFETs. So, we have performed Monte Carlo analysis to analyse the behaviour of the output with variations in threshold voltage. Fig.2 shows the DC output of the CMOS analog multiplier with the output represented in all four quadrants for bipolar inputs. The constant slope straight line shows the perfect multiplication of the two input signals V_x and V_y. Range of V_x is represented on the horizontal axis and each slope of the straight line can be identified by the value of V_y in Fig.2. From Fig.2, a particular value of one signal if varies another signal, we can find out the output at Y axis. If the slope of the line change or if it becomes saturated it indicates that the output has distortions. After getting output by applying Monte Carlo analysis, we observe that output will be distorted, and the

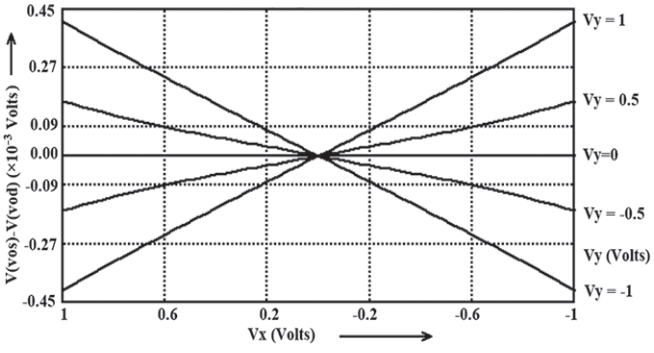

Figure 2: DC output of the CMOS Multiplier

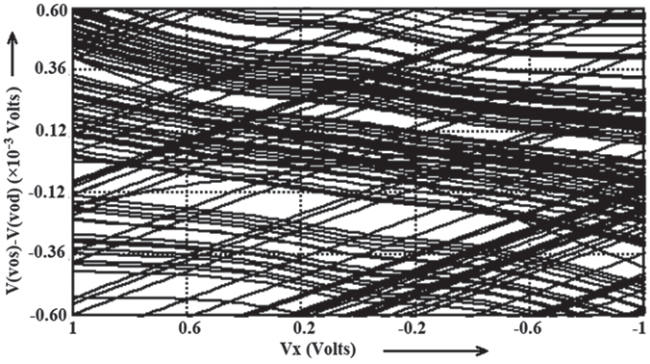

Figure 3: Monte Carlo output of the CMO Smultiplier (100 cases)

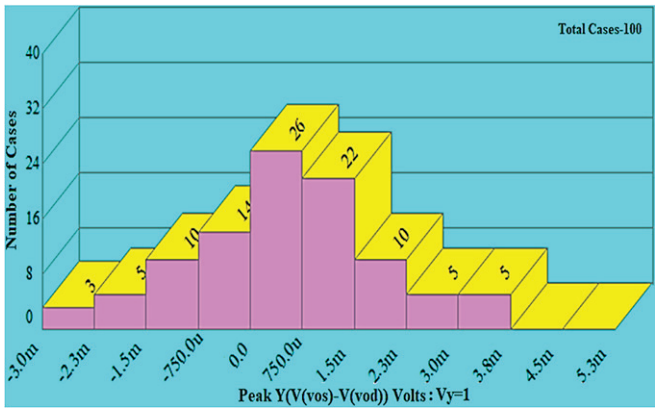

Figure 4: Output of the multiplier (2% V_{th} variation)

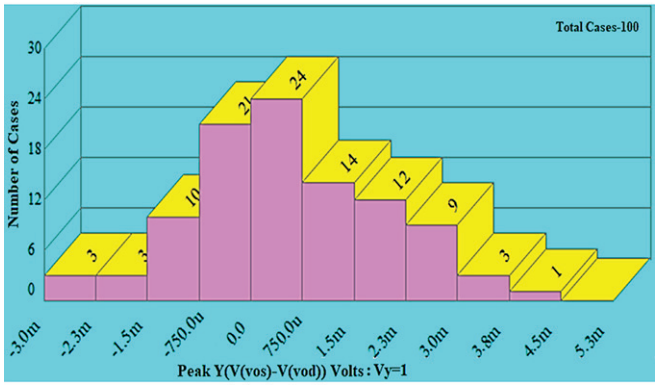

Figure 5: Output of the multiplier (5% V_{th} variation)

Table 2: Variability in circuit parameters of the CMOS multiplier (runs=100)

Distribution	Parameter V(vos)-V(vod)	Low	Mean(μ)	High	Std. Dev. (σ)
Uniform	Vth (2%)	-2.4m	513.1u	3.6m	1.4m
	Vth (5%)	-2.8m	518.8u	4.4m	1.4m

distortions increase with variations in threshold voltage. Variability is observed through the histogram plot and mean, and standard deviation of the multiplier output is reported. Fig.4. Shows the output of the multiplier (2% V_{th} variation) and Fig.5 shows the output of the multiplier (5% V_{th} variation) for 100 cases. Variations in the multiplier output has been reported under 2% and 5% variation in threshold voltage of the 65 nm bulk BSIM model. Using the case of Gaussian distribution – Monte Carlo simulation, the standard deviation in the multiplier output is found to be 1.4mV for both 2% and 5% variation. A good yield prediction with variation of 2% and 5% in V_{th} is possible at 65 nm technology node.

4.0 Conclusion

A CMOS quad multiplier has been designed using the typical design parameters to examine the variability in the performance parameters due to variations in the threshold voltage at 65 nm. V_{th} variability in CMOS circuits is implemented through Gaussian distribution - Monte Carlo analysis. Variations in the multiplier output has been reported under V_{th} variations of the 65 nm BSIM4 model. Variability is observed through the histogram plot and mean, and standard deviation of the multiplier output is reported. A good yield prediction is possible through the examination of multiplier output when the V_{th} is a varied (2% and 5%). The statistical representation of the performance parameters in this work will aid in making decisions on the cost, manufacturability, and reliability of the circuit.

5.0 References

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